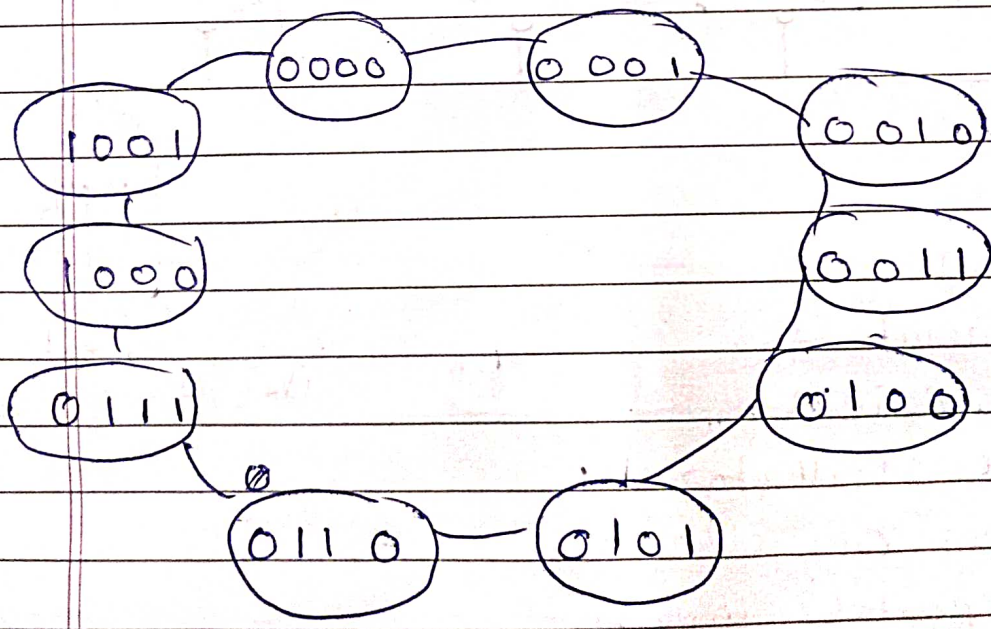
Q.2 Decade counters and also design 3 bit Asynchronous up/down counters.

Relation b/w triggring, the clock & the up-down counting imp points.

i) -ve edge triggring - Q → clock ⇒ up counter
ii) +ve " " → $\bar{Q}$ → clock ⇒ down counter
iii) +ve " " → $\bar{Q}$ → clock ⇒ Up counter
iv) +ve " " → Q → clock → down counter.

Decade counter

→ N.o. of State → 10
→ Max^m Count : 10 - 1 = 9

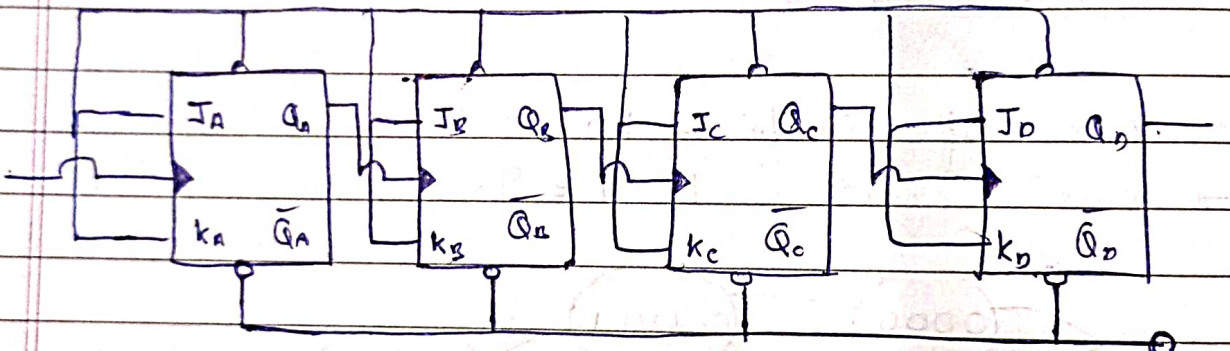


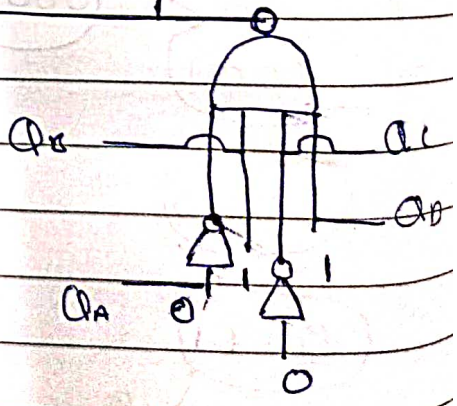
We know it's 4 bit ripple counter so 2^n is 0 to 15 but we want to stop it till 0 to 9.

Decade Counter.

Clk	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
⋮	⋮	⋮	⋮	⋮
9	1	0	0	1
10	1	0	1	0
11	1	1	1	1

→ Here we will reset our counter.





- Application
  - i) Clock generation
  - ii) Clock division
  - iii) integrated oscillator
  - iv) Low power CMOS
  - v) TTL compatible inputs
  - vi) In frequency counting circuits.